

AS1601

Dual Channel Active EMI Suppressor for Ethernet Applications

GENERAL DESCRIPTION

The AS1601 is a single-chip, highly integrated CMOS solution for Common-Mode (CM) noise suppression in Ethernet applications. Typical applications are 10/100/1000 Ethernet systems where compliance to tougher EMC standards is required.

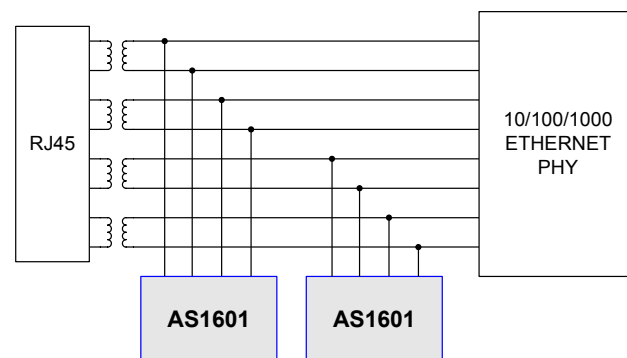
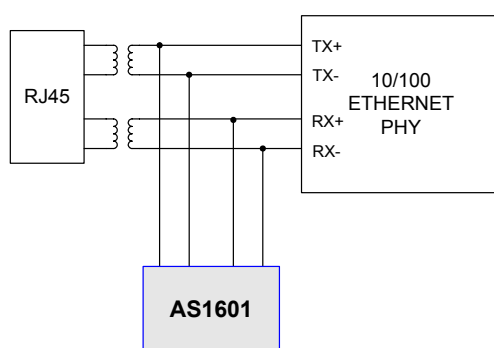
Applications include compliance to EMI Emissions (Class B), and/or EMI Immunity standards (Level 3 or higher). The AS1601 EMI Suppressor has been architected and designed to provide system level EMI suppression in Ethernet products, enabling easier path to system EMC compliance.

The AS1601 utilizes Akros Silicon's patented Active Choke technology which offers superior Common-Mode reduction and immunity compared to passive filtering techniques in Ethernet applications. The adaptive and continuous suppression operates over the entire Ethernet signal bandwidth, and it compensates for many variables that are the source of common-mode noise in Ethernet systems. It also improves the differential-to-common-mode balance of the system. This enables system designers to meet EMI emissions and EMI immunity requirements from the start of the design.

Each AS1601 supports two twisted pair interfaces. 10/100 applications require one AS1601 device while 10/100/1000 applications require two AS1601 devices. The AS1601 is available in a small footprint 16-pin QSOP Reduction of Hazardous Substance (RoHS) compliant package.

By using silicon solutions built with high-volume standard CMOS technology, Akros' customers can bring to market higher performance devices at lower cost and with a smaller footprint.

APPLICATION EXAMPLES



FEATURES

The AS1601 is fully integrated and architected at a system level to provide the following features:

- Enables system designers to comply with:
 - CISPR22 and FCC Part 15, Class B requirements for Radiated and Conducted Emissions.
 - IEC 61000-4-3/6 requirements for Radiated and Conducted Immunity, Level 3 or higher
- Provides up to 10dB of additional common-mode noise suppression over the frequency of 1MHz to 125MHz when used with Ethernet magnetics.
- Robust built-in ESD suppressors protect the Ethernet Phy and improve system ESD performance.
- JESD22-A114, ESD, HBM of $\pm 2kV$
- Interfaces to standard Ethernet transformers and 10/100/1000 Ethernet PHYs.
- Uses a single standard power rail (3.3V or 2.5V).
- Open drain output stage that can be biased from 1.8V to 3.3V using transformer center-tap supply as needed based on choice of Ethernet Phy.
- Flow-through routing for ease of board layout
- Typical power consumption of 90mW
- Low power mode available for tight power budgets
- Industrial temperature range ($-40^{\circ}C$ to $85^{\circ}C$)

APPLICATIONS

- Ethernet systems requiring additional CM suppression to meet EMC Class B emissions or higher EMI immunity requirements and ESD protection.
- POE and Non-POE Ethernet systems
- VoIP Phones, IP Cameras, WAPs, Routers, Switches
- Set Top Boxes, Networked Printers and Appliances, Desktop and Laptop Computers

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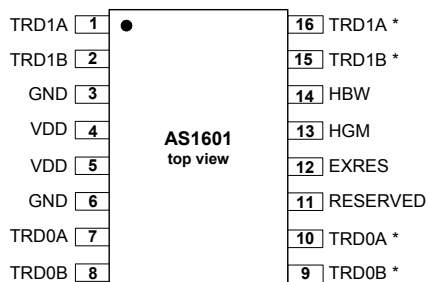
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DOCUMENT STATUS

Status:	Final Information
Revision:	1.6
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<p>Advance Information: Document contains design specifications for initial product development.</p> <p>Preliminary Information: Document contains preliminary data and will be revised at a later date.</p> <p>Final Information: Document contains specifications on a product that is in final release.</p>	

PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1. AS1601 Pin Assignments



* Not connected internally – pin named to enable PCB flow-through routing.

Table 1. AS1601 Signal Descriptions

PIN	NAME	I/O ¹	DESCRIPTION
1, 16	TRD1A	A, OD	PHY media differential pair 1 positive or negative signal. Note that circuit electrical connection is to pin 1 only. Pin 16 is named the same to enable through-routing on the PCB, however it is <i>not</i> connected internally.
2, 15	TRD1B	A, OD	PHY media differential pair 1 positive or negative signal. Note that circuit electrical connection is to pin 2 only. Pin 15 is named the same to enable through-routing on the PCB, however it is <i>not</i> connected internally.
3, 6	GND	P	Board ground - same as Ethernet PHY ground
4,5	VDD	P	Analog VDD. 3.3V \pm 5% or 2.5V \pm 5% supply can be used. VDD can be shared with transformer center-tap supply, but is not required. Note that the transformer center-tap supply voltage (VCT) must always be <i>equal to or less than</i> VDD.
7, 10	TRD0A	A, OD	PHY media differential pair 0 positive or negative signal. Note that circuit electrical connection is to pin 7 only. Pin 10 is named the same to enable through-routing on the PCB, however it is <i>not</i> connected internally.
8, 9	TRD0B	A, OD	PHY media differential pair 0 positive or negative signal. Note that circuit electrical connection is to pin 8 only. Pin 9 is named the same to enable through-routing on the PCB, however it is <i>not</i> connected internally.
11	RESERVED	-	Reserved - leave open
12	EXRES	A	External bias resistor. For VDD = 2.5V use 8.06k Ω \pm 1%. For VDD = 3.3V use 10.7k Ω \pm 1%. Connect resistor between EXRES pin and GND
13	HGM	DI	Allows trade-off between desired CM rejection performance and device power consumption: FLOATING: Default setting - recommended normal operating condition LOW: Lower power mode setting - reduces CM rejection performance to reduce power consumption. See "Performance/Power Control Pins" on page 10 for additional details. HIGH: Reserved - should not be used
14	HBW	DI	Allows control of CM rejection performance by changing internal loop bandwidth. May be used in some systems to optimize EMI performance. FLOATING: Default setting - recommended normal operating condition LOW: Reserved - should not be used HIGH: Increases loop bandwidth to increase CM rejection performance. May be used in some systems to optimize EMI performance. See "Performance/Power Control Pins" on page 10 for additional details.

1. OD = Open Drain, A = Analog signal, DI = 3-state Digital Input signal, P = Power

TEST SPECIFICATIONS

Table 2. Absolute Maximum Ratings

CAUTION: Exceeding the maximum ratings specified in this table may cause permanent damage to the device..

PARAMETER	MAX	UNIT
PHY media TRDn pins	5.0	Volt
All other pins	3.6	Volt
Supply voltage (VDD)	3.6	Volt
ESD human body model (JESD22-A114)	2	kV
ESD charged device model (JESD22-C101)	500	Volt
Storage temperature	165	°C
Junction temperature	125	°C

Table 3. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	3.3 V Power supply (VDD)	3.13	3.3	3.47	Volt
	2.5V Power supply (VDD)	2.37	2.5	2.63	Volt
VCT	DC common mode of Ethernet signals (transformer center-tap supply - see note 1)	1.8 -5%		3.3 +5%	Volt
TA	Operating temperature range	-40	–	85	°C

1. The transformer center-tap supply voltage (VCT) must always be *equal to or less than* VDD.

Table 4. Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP ¹	MAX	UNIT
Differential signal insertion loss	0.1 MHz - 100 MHz	–	0	0.2	dB
Differential output capacitance (between TRDnA and TRDnB pins)	–	–	4.5	–	pF
Common mode Phy noise rejection (25Ω CM impedance)	at 1 MHz	30	–	–	dB
	at 100 MHz	10	–	–	dB
Common mode Phy noise rejection additive to transformer ³	At 100 MHz	10	–	–	dB
Differential IM3	60 MHz full scale with 100Ω differential resistor across terminals	–	-40	–	dB
Common mode-to-differential mode imbalance	1 MHz - 100 MHz	–	-34+19.2log (f/50 MHz)	–	dB
Power dissipation	Default mode: HGM = floating V _{DD} = 2.5V, V _{CT} = 1.8V	–	90	130 ²	mW
	Low Power Mode: HGM = Low V _{DD} = 2.5V, V _{CT} = 1.8V	–	55	80 ²	

1. Typical specifications are for TA = +25°C and VDD = 2.5V. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

2. Maximum power consumption is with +5% supplies and over all process/temperature range.

3. This measurement is done with typical Ethernet transformer. Unless otherwise specified, all other performance measurements are for standalone AS1602 without Ethernet transformer.

Table 5. Digital Input Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IH}	Input HIGH level	V _{CC} = 2.5V	1.78	3.47 (3.3V + 5%)	V
		V _{CC} = 3.3V	2.0	3.47 (3.3V + 5%)	
V _{IL}	Input LOW level	V _{CC} = 2.5V	-0.30	0.5	V
		V _{CC} = 3.3V	-0.30	0.5	
I _{IL} , I _{IH}	Input leakage, LOW and HIGH levels	V _{CC} = 2.5V	±25	±40	μA
		V _{CC} = 3.3V	±33	±53	

TYPICAL CHARACTERISTICS

Figure 2. Common Mode Rejection with Typical 2-Core PoE Compatible Transformer using 3-Wire Phy-Side Choke

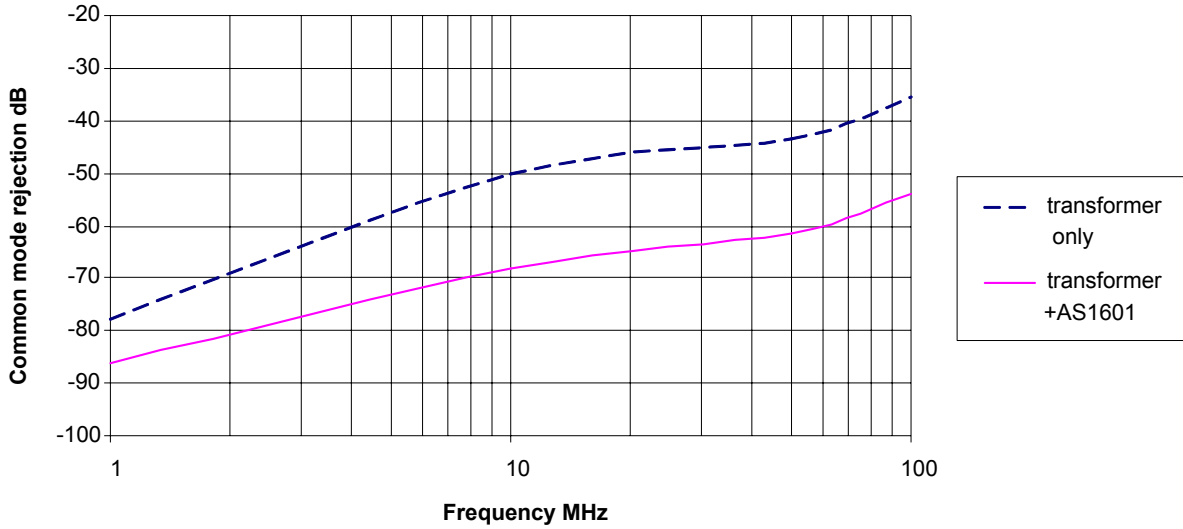


Figure 3. Common Mode Rejection with Typical 3-Core PoE Compatible Transformer with Media Side Chokes

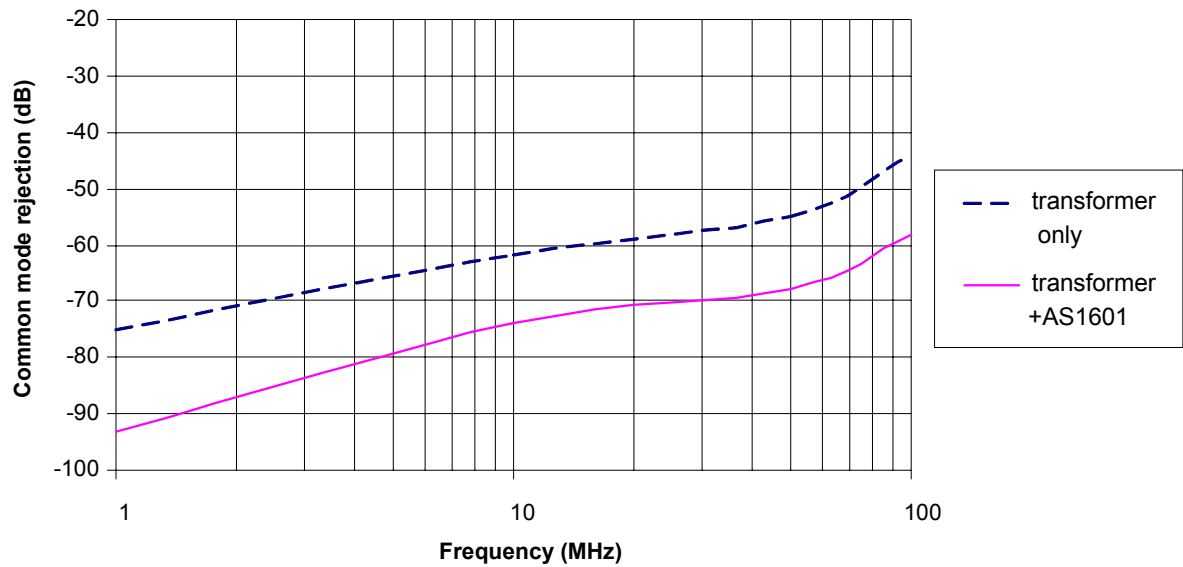


Figure 4. DM-CM Conversion in Receiving Data from UTP with Typical 2-Core PoE Compatible Transformers using 3-Wire Phy-Side Choke

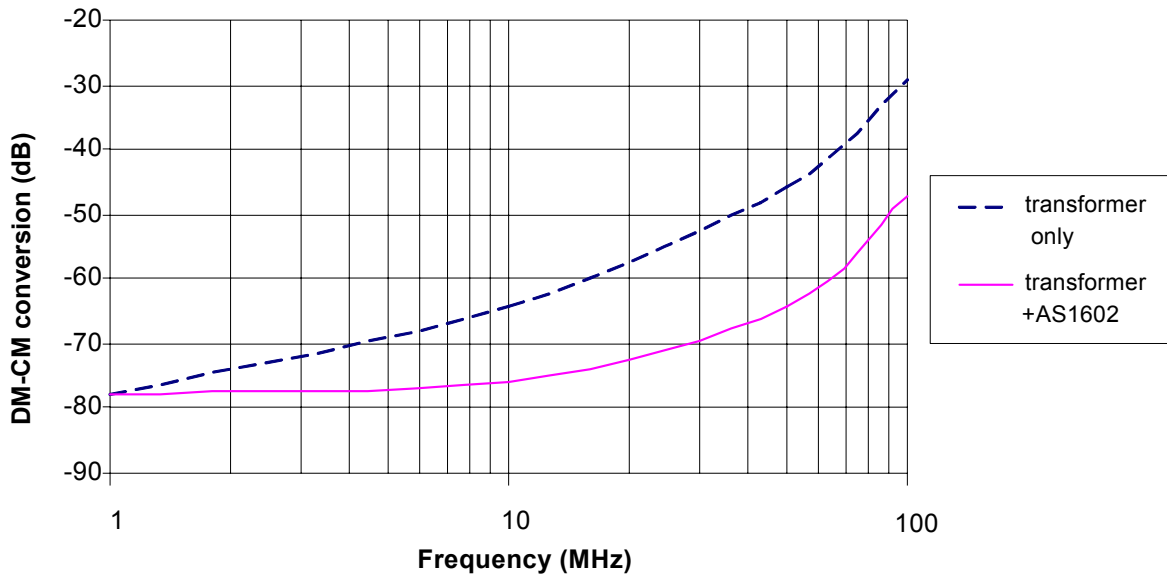


Figure 5. AS1601 Return Loss with Typical 3-Core PoE Compatible Transformer with Media Side Chokes

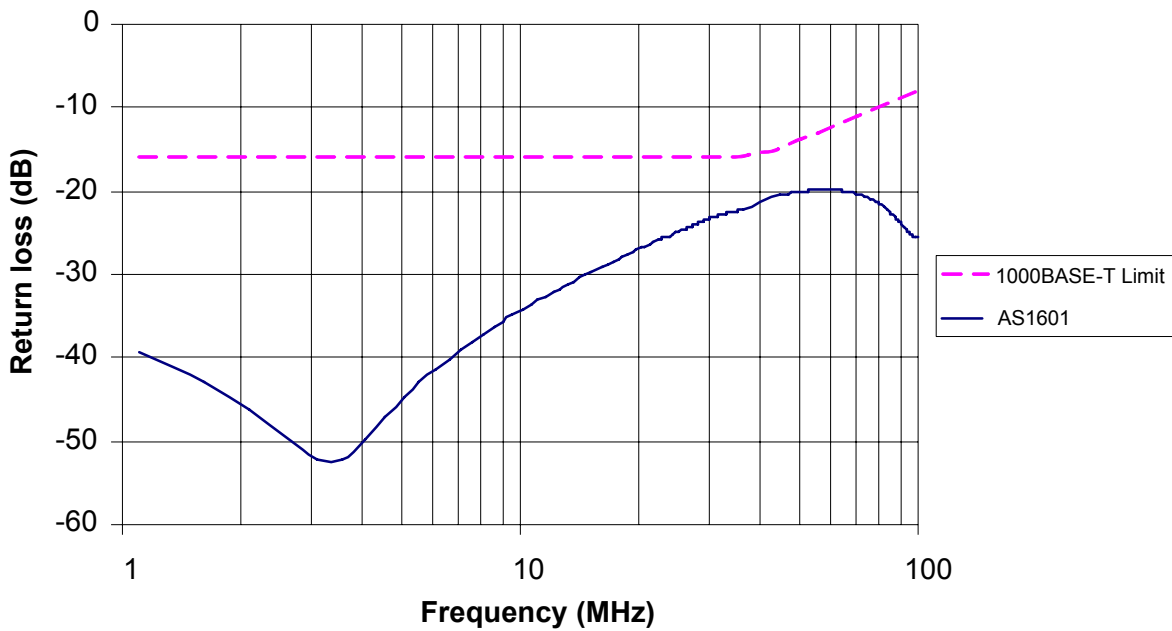
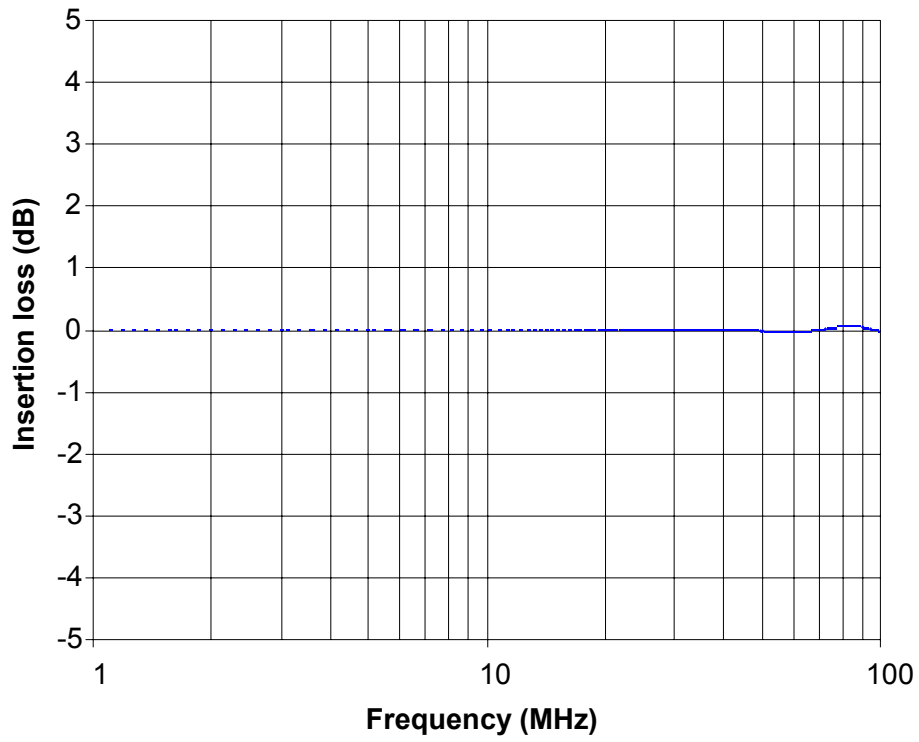


Figure 6. AS1601 Insertion Loss



FUNCTIONAL DESCRIPTION

Common Mode Noise

The AS1601 compensates for many variables that are the source of common mode noise in Ethernet systems. These include: common mode noise from Ethernet Phy DACs and drivers, variations in Ethernet line signals caused by transformer and passive component mismatches, variations in PC board designs, and different Vendor PHY designs.

Most Ethernet Phys use switched mode D/A converters and drivers to transmit complex modulated signals on the twisted pair. There are inherent common mode switching transients that occur in output driver designs. Switched mode drivers coupled with leakage inductance of the line transformer creates a common mode kick. This common mode noise is coupled through to the twisted pair line via transformer interwinding capacitance. This can result in a significant EMI emissions issue for Ethernet systems that desire good margin from CISPR22 and FCC part 15 Class B specifications.

Ethernet transformers provide common mode rejection through Phy-side autoformer and in-line chokes. Mismatches in the autoformer inductance can lead to differential-to-common mode conversion. Parasitics of the autoformer also limit common mode rejection capability. This residual common mode noise is coupled to the line side through interwinding capacitance.

Additional differential to common mode conversion issues come from board layout mismatches and other passive component mismatches on the PCB. Common mode imbalance at the input of the system can create common mode to differential conversion and significantly impact EMI immunity performance.

As a result, meeting system level EMI requirements is very challenging.

Active Choke Technology

The AS1601 incorporates Akros Silicon's patented Active Choke technology. The AS1601 is placed between the Ethernet Phy and the line transformer. Its adaptive circuitry monitors both the positive and negative signals of each differential pair and shunts any common mode noise to ground. As a result, noise is prevented from getting through the transformer to the unshielded twisted-pair (UTP).

The AS1601 preserves the integrity of the Ethernet signal by providing very low common mode impedance while maintaining high differential impedance and low differential capacitive loading.

The AS1601 is designed to suppress any common mode noise present in the Ethernet signal pair, irrespective of whether it originates from the Phy side or the UTP side. It provides immunity against large signal common mode events by shunting the common mode signal currents back to ground.

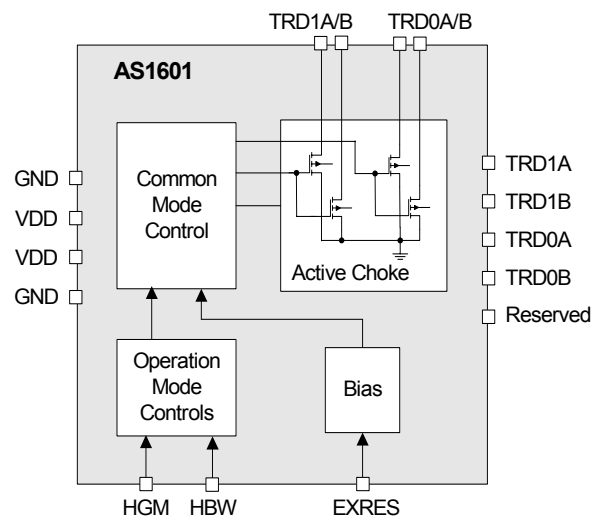
Therefore, the Ethernet Phy receiver does not see any common mode movement, enabling it to maintain good link performance.

As shown in Figure 7, the output stage of the AS1601 uses open-drain drivers similar to the most common Ethernet Phys. The AS1601 can tolerate output DC common mode on its TRD pins within a range of 1.8V to 3.3V. This allows the AS1601 to work seamlessly with any Ethernet Phy and transformer that uses the center-tap to DC-bias the Phy.

The AS1601 architecture uses high precision active analog circuitry which suppresses only the common mode components of the disturbances without impacting the differential signal. This technology provides superior differential-to-common mode impedance balance over traditional transformer solutions.

The AS1601 provides low differential capacitive loading to the Ethernet signals and meets all the common mode-to-differential balance and distortion requirements per the 10/100/1000 Base-T section of the IEEE® 802.3 Ethernet specification.

Figure 7. AS1601 Block Diagram



Performance/Power Control Pins

EMI performance varies significantly from system to system. The AS1601 provides two digital pins (HGM and HBW) that allow various levels of hardware control and performance optimization of the device. The HGM and HBW are 3-input state pins (Low, High and Floating). The Floating state is detected internally by the device as a valid state. For default operation, both pins should be left floating. These pins can be driven by another digital IC with tri-stateable outputs or tied in hardware to configure the desired operating mode.

HGM Pin

The default configuration is to leave the HGM pin floating which provides a trade-off between CM rejection performance and device power consumption.

If less rejection is needed in the Ethernet path, the HGM pin should be pulled LOW to select the Low Power Mode. In Low Power Mode, device power consumption is reduced by about 40% and CMRR performance is reduced by approximately 1dB at 100MHz.

HBW Pin

Setting the HBW pin HIGH selects HBW mode which allows system designers another dimension to improve performance by increasing the bandwidth of the internal active circuits. In some systems, this can provide additional performance benefits.

There is a broad range of line transformers that can be used in Ethernet applications. Setting HBW mode may cause oscillations in some systems depending on transformer parasitics. Therefore, HBW mode should only be used if the performance improvement of the default setting (HBW pin = Floating) is not adequate. Ethernet electrical performance should be tested sufficiently to ensure that no oscillatory behavior is seen when using the HBW mode setting.

HBW mode will typically improve the CMRR performance by approximately 1dB at 100MHz.

Note that the HBW mode can be used in conjunction with the HGM pin's Low Power mode.

Additional performance/power modulation can be achieved by changing the external bias resistor value (EXRES). For detailed characterization across operating modes, please refer to the relevant application note document.

SYSTEM DESIGN & LAYOUT CONSIDERATIONS

AS1601 Placement

AS1601 is designed to mate closely with Ethernet magnetics for ease of board design. The AS1601 should be placed physically near the Ethernet transformer or Mag-jack™. Placement on same side of the PC-board as the transformer and the Phy is recommended to avoid vias on the Ethernet traces. The AS1601 should be placed such that pin 1 is facing the transformer or mag-jack.

Ethernet Signal Polarity Interchangeability

The AS1601 extracts only the common mode component of the Ethernet signals for processing. As a result, the polarity of the Ethernet signals to the AS1601 does not matter. This allows system designers to connect either the positive or negative polarity Ethernet signals to either the TRDnA or TRDnB pins - whichever is convenient for board routing and avoids the necessity of swapping the signals and the use of via insertions.

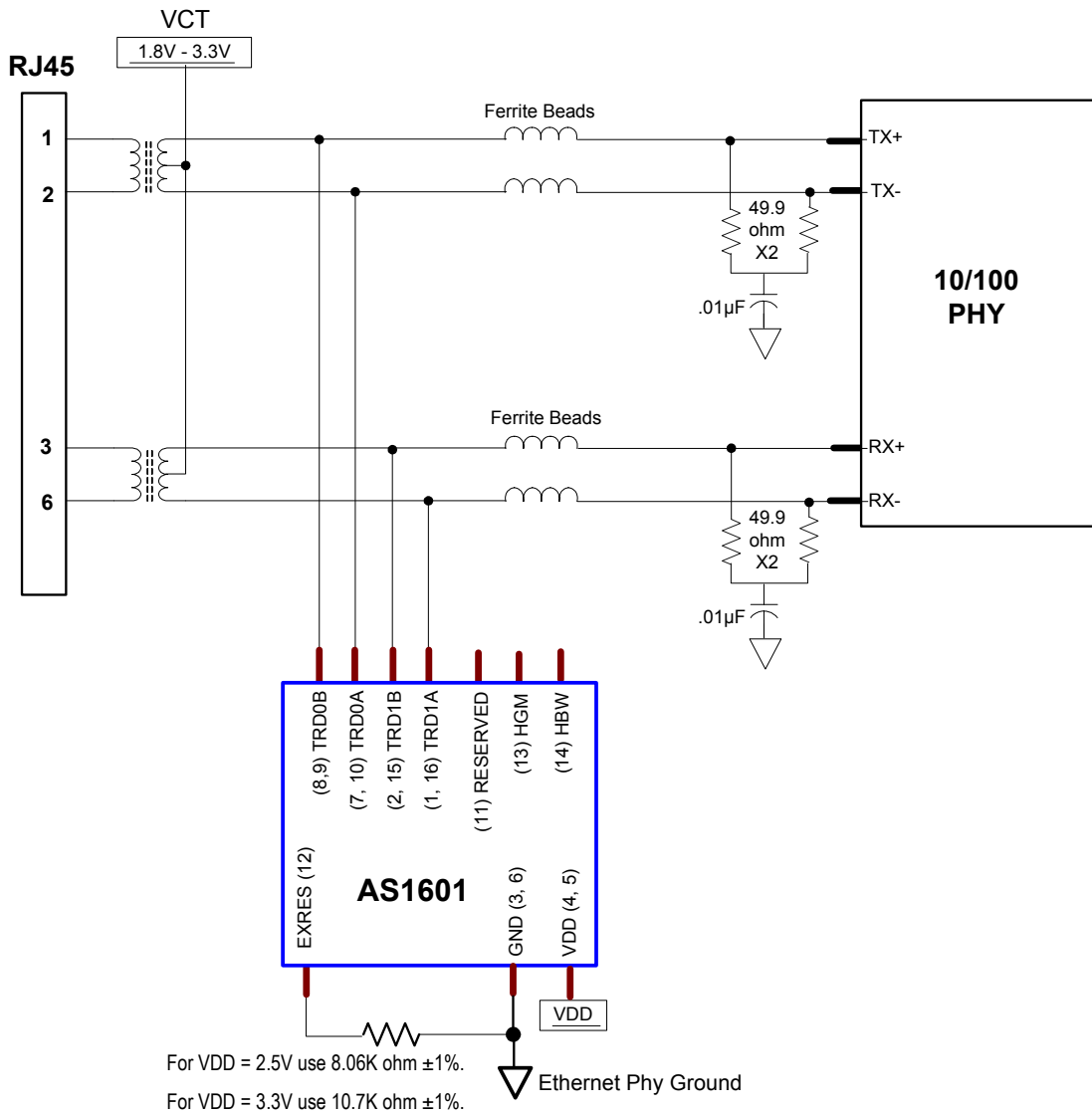
Ethernet Signal Flow-Through Routing

AS1601 is packaged to allow flow-through routing of the Ethernet differential pairs. Only one side of the package's Ethernet pins (1, 2, 7 and 8) are internally electrically connected to the CM rejection circuitry. Mirrored pins (16, 15, 10 and 9 respectively) are given the same name to enable easy flow-through routing with PC-board design tools.

For a more detailed discussion on designing with the AS1601 and layout considerations, please reference available design guide and application notes.

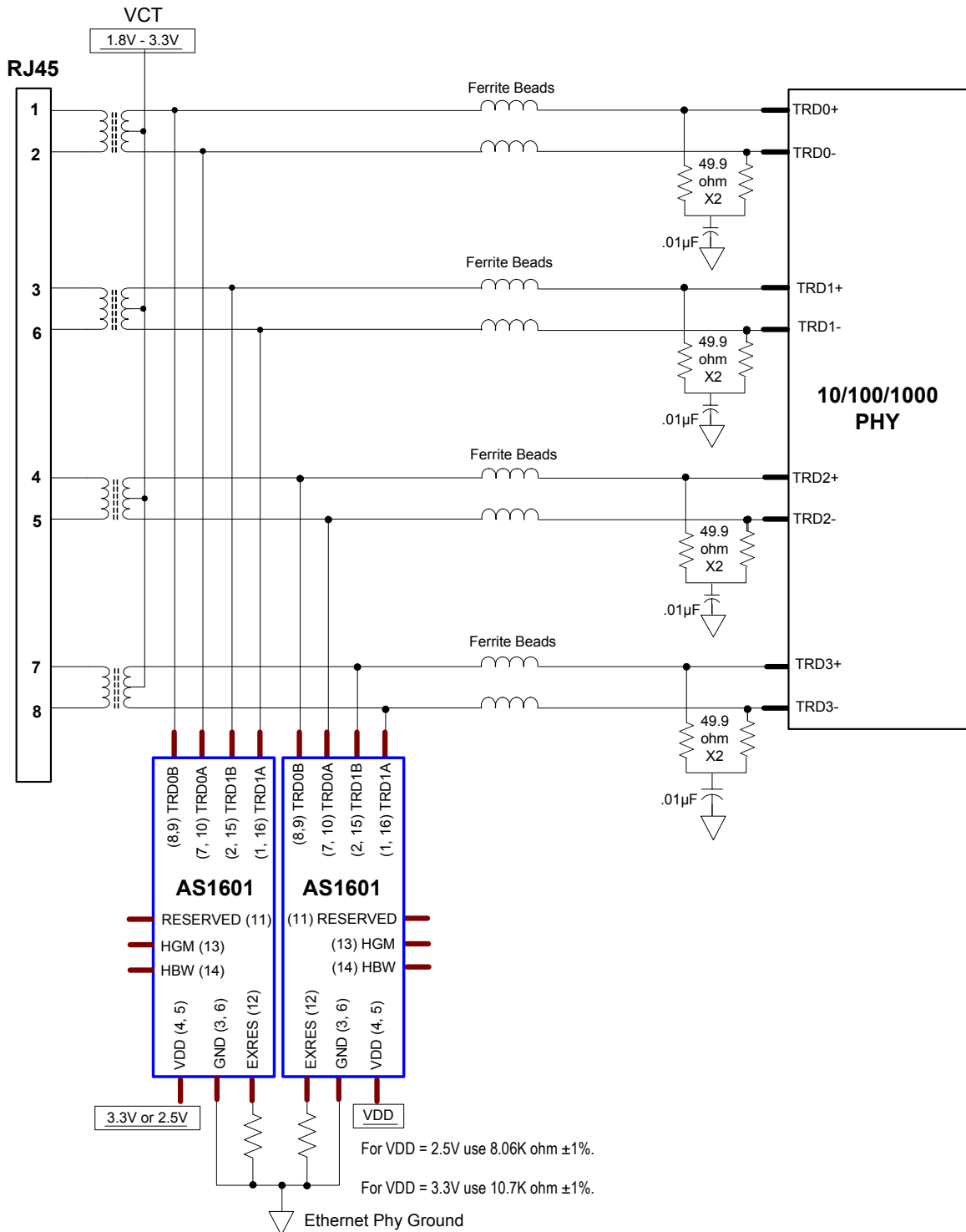
APPLICATION INFORMATION

Figure 8. Typical FE Application Circuit



NOTE: This diagram is preliminary and subject to change at any time. It may not contain all information necessary to implement the application it represents. Please refer to application notes for details.

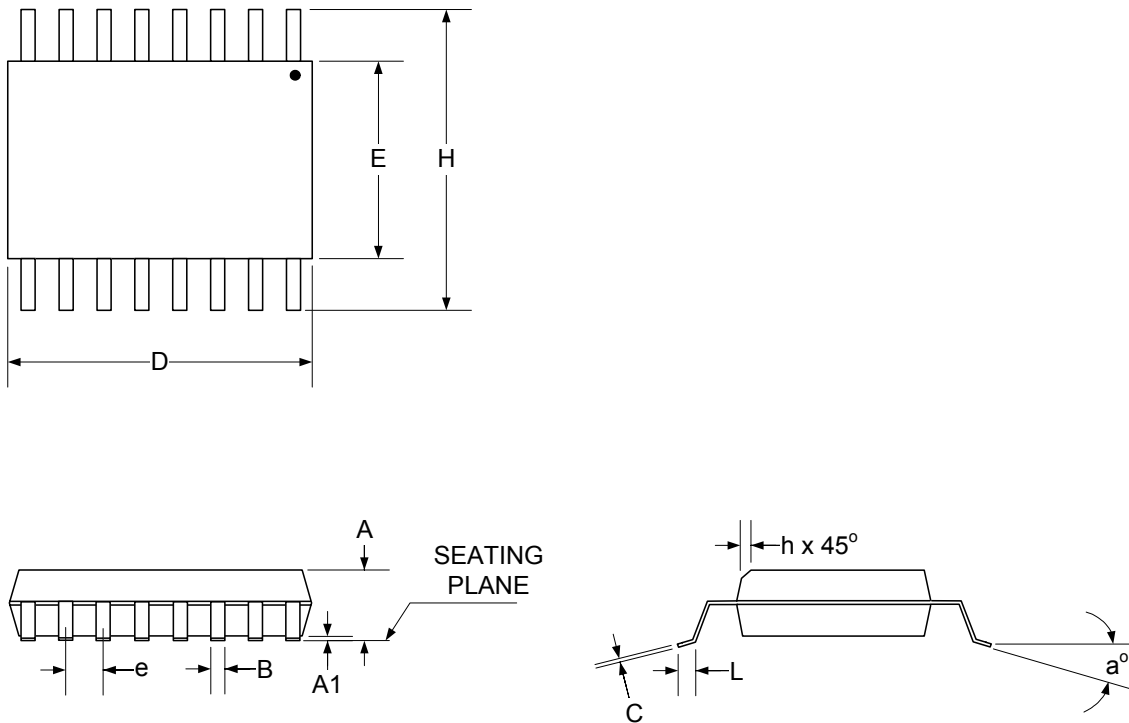
Figure 9. Typical GE Application Circuit



NOTE: This diagram is preliminary and subject to change at any time. It may not contain all information necessary to implement the application it represents. Please refer to application notes for details.

PACKAGE SPECIFICATIONS

Figure 10. 16-Pin QSOP (150 Mil) Dimensions



SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN	MAX
A	0.060	0.068	1.35	1.75
A1	0.004	0.008	0.101	0.203
B	0.009	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.188	0.197	4.80	5.00
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.254	0.38
L	0.023	0.029	0.58	0.74
a°	0°	8°	0°	8°

NOTES:

1. Lead width and lead thickness exclusive of solder plate.
2. Package outline exclusive of mold flashes and burr dimensions.
3. Allowable mold flash is 5 Mils per side.
4. Lead coplanarity is 0.003 inch maximum.

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NOTES: